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OVERVIEW ON BOOSTED CMOS DIFFERENTIAL LOGIC AND ITS APPLICATIONS

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ABSTRACT
This paper describes a boosted CMOS differential logic known as BCDL used in high speed applications where conventional CMOS logic style fails. It improves the speed performance and minimizes area by boosting the gate source voltage along the path of critical time signal. In designing a ripple carry adder, array multiplier and FIR filter and in other applications BCDL provides better speed performance which is the main concern of today's CMOS digital circuits

Keywords: Adder, Time signal, FIR Filter, Voltage Boosting, Multiplier.

I. INTRODUCTION
Bootstrapping is an important method of improving speed and reduction of power. One of the popular technique to reduce the power consumed by a CMOS digital circuit is supply voltage scaling. This is because of factor of the switching power absorbed by the circuit has a quadratic relationship with supply voltage. In some cases, the circuit is made in such a way to operate in the sub threshold region for getting maximum energy efficiency. However this approach is limited and taken in a design of low end in which speed is taken as the secondary idea because ofsevere speed degradation due to small switch current and variation of high performance because of the variations in process, temperature and threshold voltage To design a medium and high end in which performance of the efficiency related to speed and energy need importance, no acceptance of large boosted scaling of voltage and a close threshold voltage design is perfect for achieving high energy efficiency in the absence of severe speed degradation. The technique of voltage scaling helps in decreasing the total power consumed by a system. In certain applications where high speed is essential differential cascade voltage switch is avoided because of insufficient speed of the circuit. Furthermore, domino logic is not opted due to the decrease in overdrive voltage.As the scaling of supply voltage reaches the threshold voltage the performance of the speed of earlier CMOS circuits like static CMOS logic, differential cascade voltage switch (DCVS) logic [see Fig. 1(a)] and CMOS domino logic [see Fig. 1(b)] is degraded due to the decrease in overdrive voltage (VGS – VTH) of transistors. To reduce this problem, a bootstrapped CMOS having large capacitive load driver was introduced. It was a alternative to problem of speed degradation. It can increase the switching speed at supply voltage which is low using the voltage of some inner nodes goes boosted beyond the supply rails. In this method two capacitors are used for the aim of bootstrapping. However this circuit was introduced as a driver of large capacitive load, logic functions cannot be fit into the circuit and the merits of speed was not fully exploited. Operation of fast logic with low supply voltage, BDL which is known as CMOS bootstrapped dynamic logic was introduced [see Fig.1(c)]. However, the speed of this BDL was not so good due to the bulky bootstrapped circuit which was superimposed over the entire circuit. Moreover, there is a limitation of construction of logic of BDL since it is known as a one ended structure.

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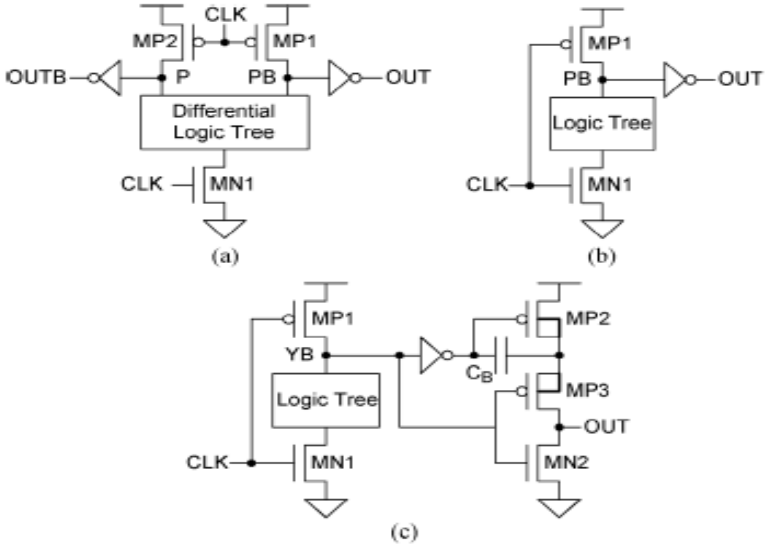


Fig. 1. Conventional digital CMOS circuits. (a) DCVS. (b) Domino CMOS logic. (c) BDL.

To eliminate the above problem BCDL known as differential logic style was introduced. It is not only good in terms of improving switching speed but also decreases area because of sharing of single boosting circuit. Switching speed is good due to the boosting of overdrive voltage along the critical timing signal path. However the problem of latency can be reduced by allowing the voltage boosting block directly to differential logic tree.

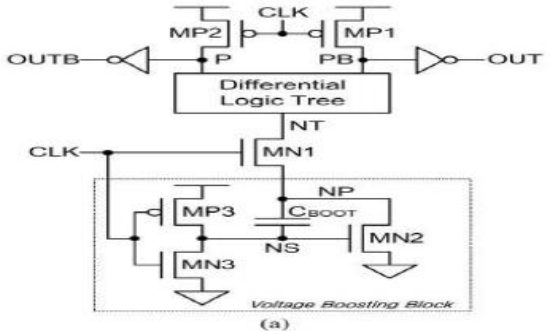
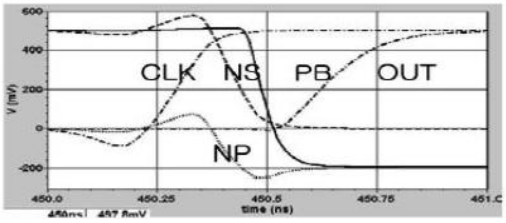


Fig. 2 (a) BCDL structure



(b) Simulated waveforms

It contains a block of differential logic known as precharged and a voltage boosting block. The lower part of the circuit is referred as voltage-boosting block which is given in the dotted box made of transistors referred as MN2, MN3, and MP3 and CBOOT known as boosting capacitor and is used in boosting the voltage of NP reaches below the ground. The logic block known as precharged differential, which contains a tree of differential logic with bottom transistor named as MN1, precharge transistors referred as MP1 and MP2 and output inverters accepts the boosted voltage at NP and calculate the value of the output logic. Its operation is in two phases referred as a precharge phase and a boosted evaluation phase. The circuit is in precharge phase when the CLK value is low. When there is a precharge phase, there is a separation of the precharge differential logic block from the voltage boosting block due to the turn of MN1. Precharge nodes referred as P and PB which are in the differential logic block are precharged to the supply voltage with the assistantship of MP1 and MP2 resulting in outputs named as OUT and OUTB low. On similar time, turn on of the transistors known as MP3 and MN2 which are in voltage boosting block resulting NS to high and NP to low. Then a voltage that is identical to the supply voltage is applied to CBOOT. When there is a change of CLK low to high then the circuit appears into the phase of boosted evaluation. The waveform executed in this phase of BCDL are shown in Fig. in which supply voltage of 0.5V is used. When there is a change of CLK to high then MN1 turns on and the operation of connection of the differential logic tree to the voltage boosting block is taking place. During this time there is a pull down of NS toward the ground that result in boosting of NP and NT below the ground with

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the help of capacitive coupling carried by CBOOT. As given in Fig. , NP temporary approaches at -250 mV and settles at near -200 mV by the boosting action. Then the gate to source voltage of MN1 and transistors in the logic increases driving strength of all these transistors. However, a small forward in the source body voltage introduced in these transistors that uses boosting source voltages reachesbelow the ground leads to a decrease in threshold voltage of all these transistors, furthermore, increasing their driving strength. However the boosted voltage approaches at NT is then appears to P or PB is pulled down below the ground. Then, there is an enhancement in the gate source voltage of the driver PMOS transistor enhances its driving strength. Effects of all these driving strength that is carried out by boosting process are then combined together along the path of critical timing signal taken from input to output through the nodes of precharging that leads to improvement in switching speed at a low voltage region.Thus it helps in increasing switching speed and considered as a good differential logic style that is utilized in high speed applications.

II. APPLICATIONS

1. Ripple carry adder

Ripple carry chain consists of 8 bit was used in the BCDL adder which main function is to boost the operation of each carry chain stage Meanwhile a carry chain of 8 bit Manchester was used in the adder of DCVS and BDL for propagation of carry of high speed. Fig.3 shows the conventional structure of 8 bit ripple carry chain used in the BCDL adder.

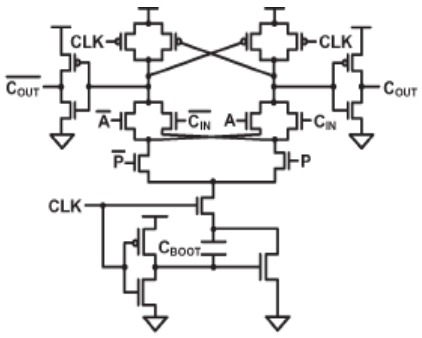

Fig.3. Conventional structure of 8 bit ripple carry chain used in BCDL

XOR gate

Carry is propagated with the help of XOR gate when the value of both inputs are 1 whereas it is generated when the value of either of its input are 1. Fig.4 shows the structure of xor gate used for carry propagation.

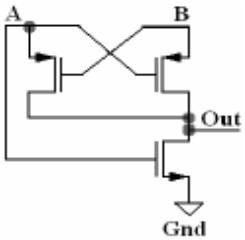

Fig. 4. XOR gate

$P_i = A_i$ xor B_i (1)

The proposed 8 bit ripple carry chain used in the BCDL is shown in Fig. 5

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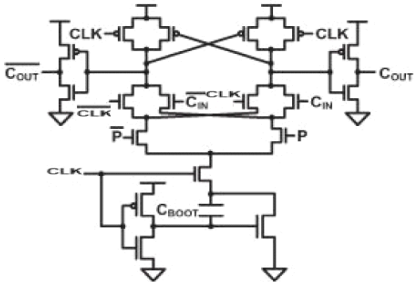

Fig5. Proposed 8 bit ripple carry chain in BCDL

2. BCDL logic fir filter

With the logic of BCDL, FIR filter can be designed. It consists of adder, delay element and array multipliers. Fig.7 shown below is a BCDL logic FIR filter. In place of h (0), h (1), h (2), h (3), h (4) array multiplier can be designed.

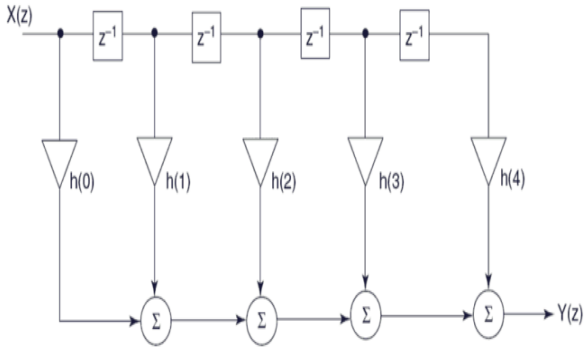

Fig.7 BCDL logic FIR filter

BCDL provides lower energy delay product and takes reduction in addition time when designing an FIR filter.

3. Array multiplier

BCDL can also be used in designing a array multipliers. This high speed arraymultiplier when used in designing a high speed performance FIR filter gives high speed performance. Fig.8 shows 32x32 array multipliers

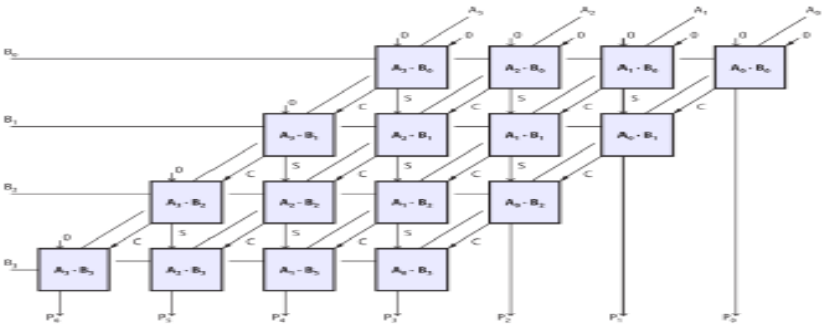

Fig.8 32x32 array multiplier

III. CONCLUSION

CMOS differential logic style having feature of voltage boosting has been described. The BCDL gives increased switching speed when compared to conventional logic style at low supply voltage using a single boosting circuit that isshared by complementary outputs. The BCDL also reduces the area. Need of portable digital devices is high speed performance and low power dissipation. BCDL when used in applications provides all these features when compared to conventional logic styles. BCDL applications which are used in Ripple carry adders, FIR filter and array multiplier has been described.

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